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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/784,577	02/23/2004	Donald Thomas McGrath	RD-27645-2	9571

7590 12/15/2004

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EXAMINER	
SHINGLETON, MICHAEL B	

ART UNIT	PAPER NUMBER
2817	

DATE MAILED: 12/15/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/784,577	MCGRATH, DONALD THOMAS	
	Examiner	Art Unit	
	Michael B. Shingleton	2817	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 5-9 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 6-9 is/are rejected.

7)☒ Claim(s) 5 is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Being that the instant application is a divisional and it is noted that in the preliminary amendment applicant recites that "Claims 1-20 are pending in this application", it is clearly apparent that claims 21-24 are cancelled. Thus, for examining purposes it is assumed that these claims are cancelled. Applicant also recites in the preliminary amendment that "Claims 1-4...are canceled." Claim 5 is dependent on cancelled claim 2, but it is clearly apparent that applicant meant to cancel this claims as well. However, for examining purposes claim 5 is objected to because of its dependency on cancelled claim 2 (Note below.) Please clarify these two issues.

Claim 5 is objected to because of the following informalities: Claim 5 is dependent on cancelled claim 2. It appears that applicant meant to cancel this claim, however, because of the dependency on cancelled claim no meaningful search can be preformed on this claim. It is also possible that applicant meant to change the dependency to a pending claim and thus a mere typo has occurred. Appropriate correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Biard 4,661,726 (Biard).

Figure 4 and the relevant text of Biard discloses a buffered field effect transistor (BFL) level-shifting/inverter circuit having an input "IN", a first depletion mode inverter that receives the IN signal at a depletion mode MOSFET 30, and a buffered field effect transistor logic stage. The buffered field effect transistor logic stage has a first depletion mode MOSFET 32 and a second depletion mode MOSFET 37. A voltage drop or what is commonly called a level shifter is connected between the first and second transistors and is composed of elements like 33, 34. The node between element 32 and 33 forms a first output and the node between element 37 and 36 forms a second output. It is important to note that column 1, around line 50 does recites that the logic gates of the invention "will therefore be described in terms of such logic gates" i.e. MESFETs, but Biard is very specific that "[t]hose skilled in the art will readily perceive that the invention (which includes the BFL of Figure 4) may be used with any logic gate utilizing depletion mode FET's. Such FET's may be metal oxide semiconductor field effect transistors (MOSFET's)...(emphasis added)." Thus the Figure 4 embodiment is clearly applicable to MOSFETs and

includes depletion mode MOSFETs. Biard is silent on the type of depletion mode MOSFET, i.e. NMOS or PMOS. NMOS and PMOS depletion mode MOSFETs are conventional forms of depletion mode MOSFETs.

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have used depletion mode NMOS transistors for the transistors of Biard because, as the Biard reference is silent on the exact depletion mode FET used one of ordinary skill in the art would have been motivated to use any art-recognized equivalent depletion mode FET such as the conventional depletion mode MOSFET.

Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Biard 4,661,726 (Biard) as applied to claim 6 above, and further in view of Tohyama 4,810,907 (Tohyama).

Biard is silent on the use of resistor(s) for the voltage drop circuit.

Tohyama shows that the resistor, the diode and the "diode connected " FET like that of Biard are all art recognized equivalent voltage drop circuits for use in BFT's.

Thus it would have been obvious to one of ordinary skill in the art at the time the invention was made to have replaced the voltage drop circuit of Biard with a resistor because two voltage drop circuits are well known to be equivalent as taught by Tohyama.

Claims 8 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Biard 4,661,726 (Biard) in further in view of Tohyama 4,810,907 (Tohyama) and Alok et al. 6,559,068 (Alok).

Figure 4 and the relevant text of Biard discloses a buffered field effect transistor (BFL) level-shifting/inverter circuit having an input "IN", a first depletion mode inverter that receives the IN signal at a depletion mode MOSFET 30, and a buffered field effect transistor logic stage. The buffered field effect transistor logic stage has a first depletion mode MOSFET 32 and a second depletion mode MOSFET 37. A voltage drop or what is commonly called a level shifter is connected between the first and second transistors and is composed of elements like 33, 34. The node between element 32 and 33 forms a first output and the node between element 37 and 36 forms a second output. It is important to note that column 1, around line 50 does recites that the logic gates of the invention "will therefore be described in terms of such logic gates" i.e. MESFETs, but Biard is very specific that "[t]hose skilled in the art will readily perceive that the invention (which includes the BFL of Figure 4) may be used with any logic gate utilizing depletion mode FET's. Such FET's may be metal oxide semiconductor field effect transistors (MOSFET's)...(emphasis added)." Thus the Figure 4 embodiment is clearly applicable to MOSFETs and

includes depletion mode MOSFETs. Biard is silent on the type of depletion mode MOSFET, i.e. NMOS or PMOS. Alok discloses that silicon carbide NMOS and PMOS depletion mode MOSFETs formed on a silicon carbide substrate are conventional forms of depletion mode MOSFETs (See entire reference.). Alok also teaches the motivation for use of Silicon Carbide transistors that includes that they are ideal for "high voltage, high frequency and high temperature" (See column 1, around line 33).

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have used silicon carbide depletion mode NMOS transistors formed on a silicon carbide substrate for the transistors of Biard because, as the Biard reference is silent on the exact depletion mode FET used one of ordinary skill in the art would have been motivated to use any art-recognized equivalent depletion mode FET such as the conventional silicon carbide depletion mode NMOS MOSFET formed on a silicon carbide substrate. Additionally one of ordinary skill would have been motivated to make the combination because of the higher voltage handing, the higher frequency capabilities and the higher temperature handing capabilities as compared to conventional Si based MOS devices as taught by Alok. Silicon carbide MOSFETs are better FETs.

Biard is silent on the use of resistor(s) for the voltage drop circuit.

Tohyama shows that the resistor, the diode and the "diode connected " FET like that of Biard are all art-recognized equivalent voltage drop circuits for use in BFT's.

Thus it would have been obvious to one of ordinary skill in the art at the time the invention was made to have replaced the voltage drop circuit of Biard with a resistor because two voltage drop circuits are well known to be equivalent in the art as taught by Tohyama.

Because the combination made obvious above includes depletion mode NMOS transistors, this circuit being the same as that claimed is configured to operate with a negative direct current bias on each of the gates with respect to the associated channel.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The circuit of Ogawa et al. 6,127,857 is very close to the claimed invention and could form the basis of a 35 USC 103 rejection, but is not considered to be "better" than the applied Biard reference because it does not show the level shifting element like element 33 of Biard. However, note that it transistors 13, 14, 17 and 18 are depletion mode NMOS's (See column 11, around line 25). Kim et al. 5,313,435 shows the general state of the art as it concerns voltage drop elements like resistor 75.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael B. Shingleton whose telephone number is (571) 272-1770. The examiner can

normally be reached on Tues-Fri from 8:30 to 4:30. The examiner can also be reached on alternate Mondays. The examiner normally has the second Mondays of the bi-week off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Pascal, can be reached on (571)272-1769. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

MBS
December 7, 2004

Michael B Shingleton
MICHAEL B SHINGLETON
PRIMARY EXAMINER
GROUP ART UNIT 2817